WHAT IS CLAIMED IS:

1. A semiconductor memory device in which internal states at a time of carrying out an access operation to a memory cell have two or more different operation modes, the semiconductor memory device comprising:

a mode discriminating section for discriminating one of the operation modes at every operation cycle constituted by, as one unit, an operation period for carrying out the access operation and a stand-by period from an end of the operation period to a start of a next operation period;

a switching section for switching among the internal states; and

a switching control section for outputting a switching control signal to the switching section in accordance with a discrimination result obtained in the mode discriminating section,

in which the switching control signal is not outputted in a stand-by period before a start of the operation cycle, but is outputted in the operation period subsequent to the start of the operation cycle.

2. A semiconductor memory device according to claim 1, wherein:

the switching control section includes a recording section for holding the switching control signal outputted in accordance with the discrimination result in the mode discriminating section; and

the recording section renews the switching control signal only in a case where the discrimination result in

the mode discriminating section is different from the discrimination result in the former operation cycle.

3. A semiconductor memory device according to claim 1, wherein the switching section is always set into one of the internal states.

4. A semiconductor memory device according to claim 1, wherein:

the operation modes are access modes to the memory cell, and

the internal states are address supply paths different for each of the access modes.

5. A semiconductor memory device according to claim 4, wherein:

the access modes include a data-input/output mode and a refresh mode, and

the address supply paths include a supply path from an outside and a supply path from an internal address counter.

6. A semiconductor memory device according to claim 1, wherein:

the operation modes are access modes to the memory cell; and

the internal states correspond to the number of bits with respect to an address to be decoded different for each of the access modes.

7. A semiconductor memory device according to claim 6, wherein the number of bits with respect to the address is the number of bits from a high order bit position to a predetermined low order bit position in the address.

8. A semiconductor memory device according to claim 7, wherein:

the access modes include a data-input/output mode and a refresh mode; and

the predetermined low order bit position in the data-input/output mode is a lower order than the predetermined low order bit position in the refresh mode.

9. A semiconductor memory device having a data-input/output mode and a refresh mode as an access operation to a memory cell, comprising:

a mode discriminating circuit for discriminating between the data-input/output mode and the refresh mode at every operation cycle constituted by, as one unit, an operation period for carrying out the access operation and a stand-by period from an end of the operation period to a start of a next operation period;

a switching control circuit for outputting a switching control signal in the operation period after a start of the operation cycle only in a case where an operation mode discriminated by the mode discriminating circuit is different from an operation mode in the former operation cycle; and

an address switching circuit for switching a connection to a decoding circuit at every output of the

switching control signal, while one of an external address used in the data-input/output mode and a refresh address from a refresh address counter used in the refresh mode is always connected to the decoding circuit.

10. A semiconductor memory device having a data-input/output mode and a refresh mode as an access operation to a memory cell, comprising:

a mode discriminating circuit for discriminating between the data-input/output mode and the refresh mode at every operation cycle constituted by, as one unit, an operation period for carrying out the access operation and a stand-by period from an end of the operation period to a start of a next operation period;

a switching control circuit for outputting a switching control signal in the operation period after a start of the operation cycle only in a case where the operation mode discriminated by the mode discriminating circuit is different from the operation mode in the former operation cycle; and

a block decoding circuit in which when a memory cell array block to be accessed is specified, either a first number of bits with respect to address decoded in the data-input/output mode or a second number of bits with respect to address decoded in the refresh mode, smaller than the first number of bits is always connected, and connection is switched at every output of the switching control signal alternately between the first number and the second number.

11. A control method of a semiconductor memory device

in which address supply paths at a time of carrying out an access operation to a memory cell have two or more different operation modes, comprising:

a mode discriminating process of discriminating one of the operation modes at every operation cycle constituted by, as one unit, an operation period for carrying out the access operation and a stand-by period from an end of the operation period to a start of a next operation period; and

a switching control process of renewing a switching control signal selecting one of the address supply paths in accordance with a discrimination result of the mode discriminating process, not in a stand-by period before a start of the operation cycle, but in an operation period subsequent to the start of the operation cycle.

12. A control method of a semiconductor memory device in which activating sections of a memory cell array at a time of carrying out an access operation to a memory cell have two or more different operation modes, comprising:

a mode discriminating process of discriminating one of the operation modes at every operation cycle constituted by, as one unit, an operation period for carrying out the access operation and a stand-by period from an end of the operation period to a start of a next operation period; and

a switching control process of renewing a switching control signal selecting one of address bit numbers of the activating sections in accordance with a discrimination result of the mode discriminating process, not in a stand-by period before a start of the operation cycle, but in an operation period subsequent to the start of the operation

cycle.

13. A control method of a semiconductor memory device according to claim 11, wherein:

the switching control signal renewed in the switching control process is held; and

the switching control signal is renewed only in a case where the discrimination result of the mode discriminating process is different from the discrimination result of the former operation cycle.

14. A control method of a semiconductor memory device according to claim 11, wherein any one of the address supply paths is always established.

15. A control method of a semiconductor memory device according to claim 11, wherein at least the two operation modes include a data-input/output mode and a refresh mode.

16. A control method in which internal states at a time of carrying out an activating operation have two or more operation modes, comprising:

a mode discriminating process of discriminating one of the operation modes at every operation cycle constituted by, as one unit, an operation period for carrying out the activating operation and a stand-by period from an end of the operation period to a start of a next operation period;

a mode recording process of storing one of the operation modes discriminated in the mode discriminating process;

a comparison process of comparing one of the operation modes discriminated in the mode discriminating process with one of the operation modes of the former operation cycle stored in the mode recording process; and

a switching control process of giving a switching-procedure instruction among the internal states in accordance with the comparison result in the comparison process, not in a stand-by period before a start of the operation cycle, but in the operation period subsequent to the start of the operation cycle.

17. A control method according to claim 16, wherein in the switching control process, the switching-procedure instruction is given only in a case where a former comparison result in the comparison process is inconsistent with a present comparison result.

18. A control method according to claim 16, wherein in the switching control process, in a case where the same operation mode is set in a plurality of continuous operation cycles, the switching-procedure instruction is given only in a first operation cycle in the plurality of operation cycles.

19. A control method according to claim 16, wherein the switching-procedure instruction is an output of a control signal for setting one of the internal states in accordance with the operation mode, and

the control signal is outputted in the switching control process.

20. A control method according to claim 16, wherein:

the internal states are supply methods of an internal signal; and

switching among the internal states is switching among supply sources of the internal signals.

21. A control method according to claim 16, wherein: the internal states are decode states of an internal signal; and

switching among the internal states is switching among bit numbers of the internal signal to be decoded in the decode state.